



SHAPING THE NEXT GENERATION OF ELECTRONICS

**JUNE 23-27, 2024**

MOSCONE WEST CENTER  
SAN FRANCISCO, CA, USA

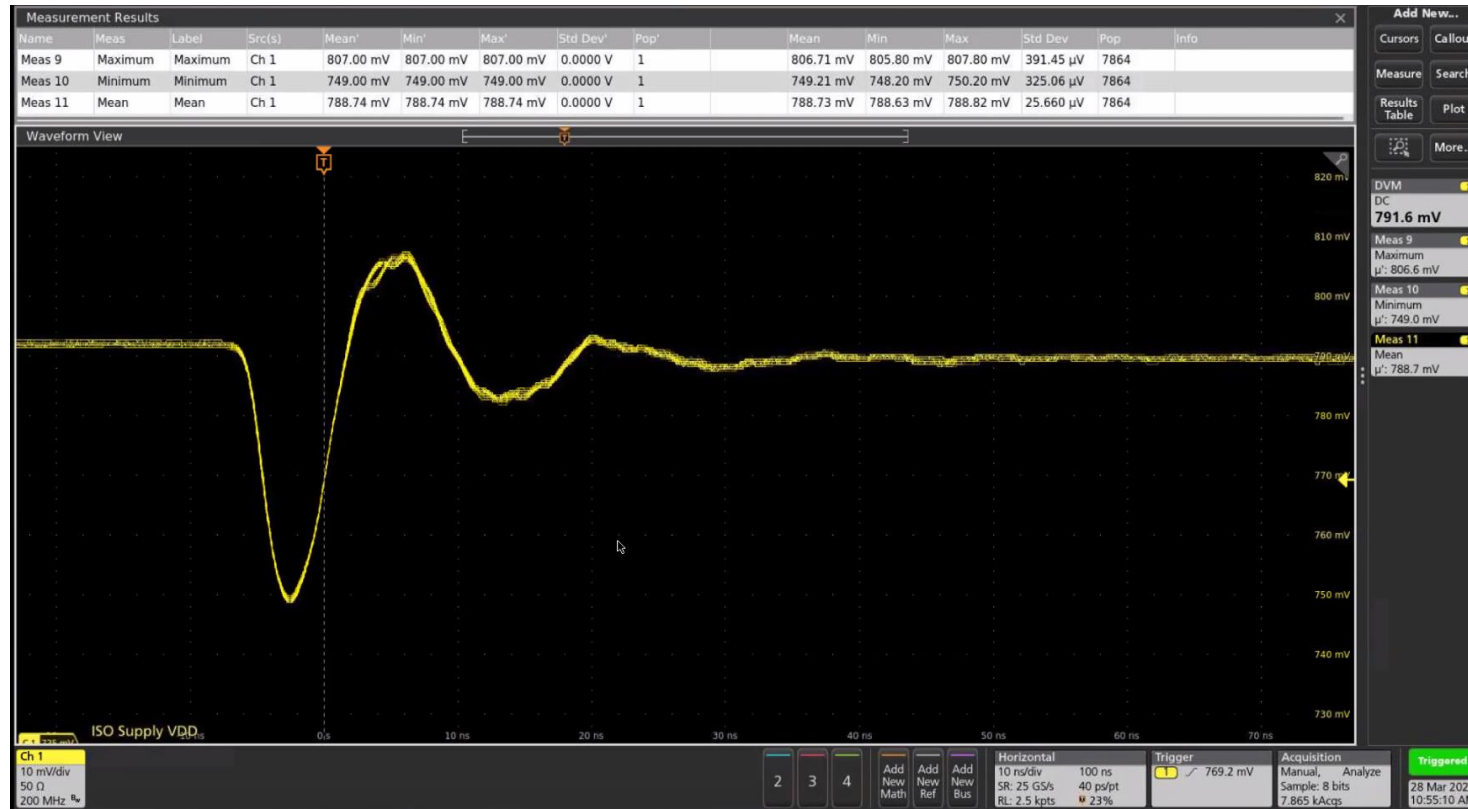
# Droop! There it is!

Michael Durr  
FAE Manager  
Movellus

MOVELLUS™



# What is Voltage Droop?

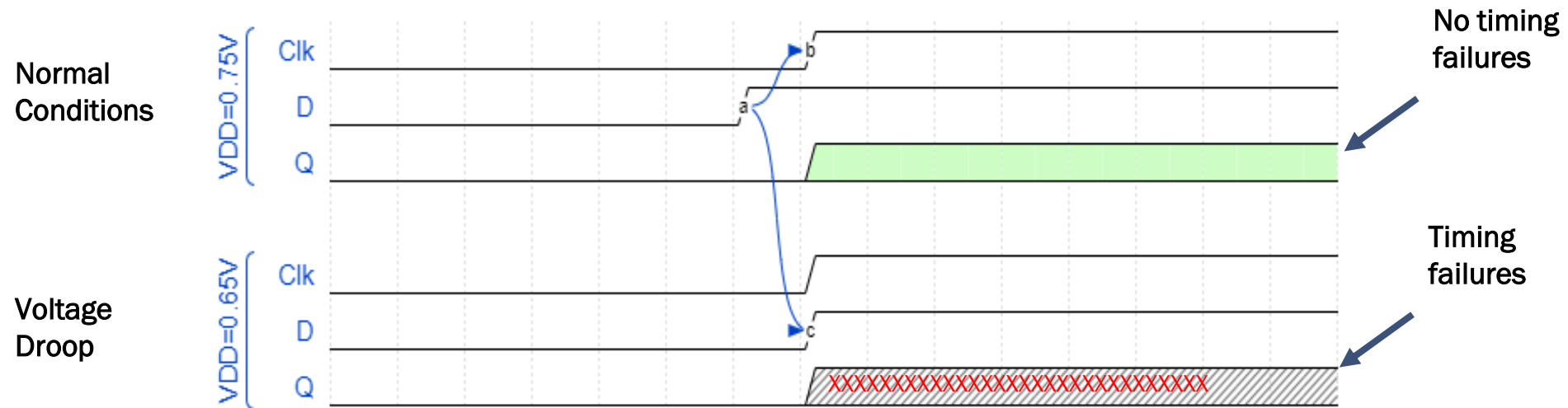


Unexpected and transient voltage fluctuation

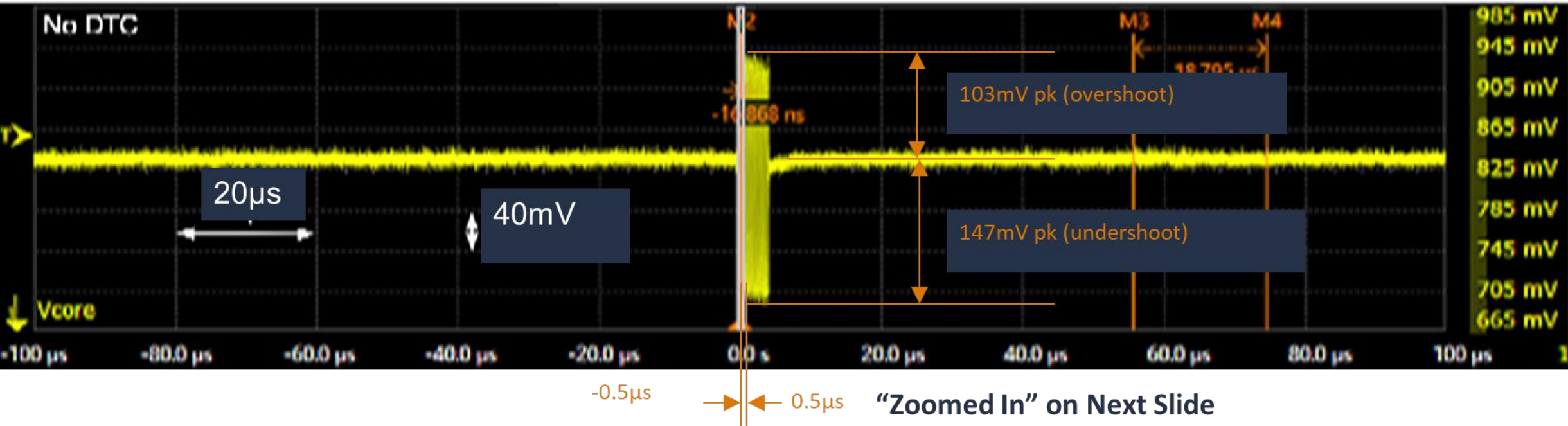
Droop Causes:

- Dynamic workloads
- Weakness in power networks
- Inadequate de-cap

# Impact of Droop in Digital Systems



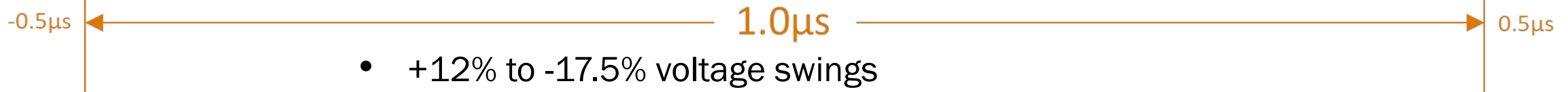
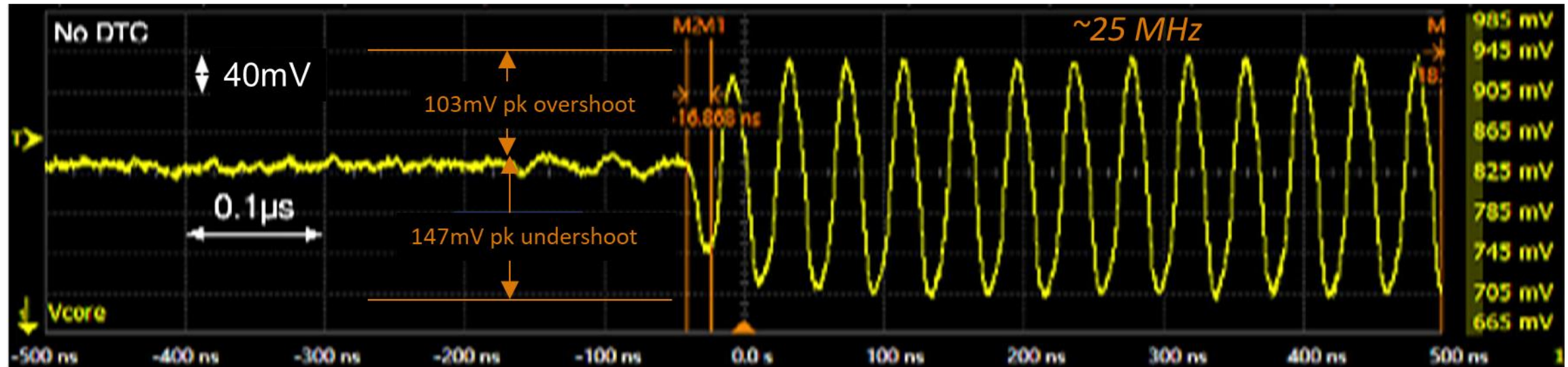
# Real World Voltage Droop Example



ISSCC 2023: 29.4 Wafer-Level Stacking of High-Density Capacitors to Enhance the Performance of a Large Multicore Processor for Machine Learning Applications



# Real World Voltage Droop Example (Zoomed In)



- +12% to -17.5% voltage swings
  - -17.5% is well below the typical -10% margin
  - +12% could have reliability issue too
  - Static IR-Drop ~3.5%

# Passive Droop Mitigation

## Increase Voltage

- Increases System Power
- Lowers Long-Term Reliability

## Decrease Frequency

- Negatively Impacts Performance

## Improve PDN

- More Routing Congestion
- Add wires & vias

# Barriers to Active Droop Mitigation



Custom  
Solutions



System  
Complexity



IP  
Interoperability

# 5 Keys to Active Droop Mitigation

**1** Fast Detect and Adapt Time

**2** Intelligent Clock Frequency Management

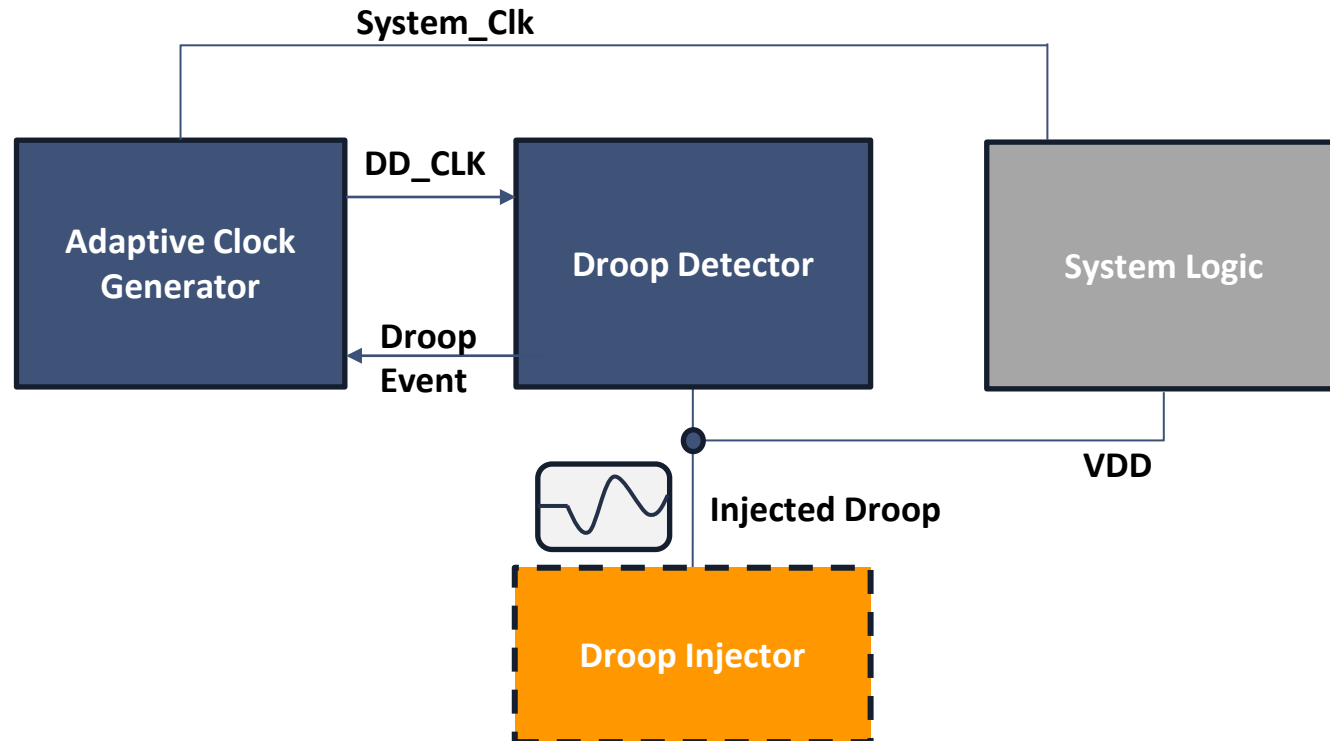
**3** Flexible and Programmable Droop Response

**4** Observability

**5** Turnkey Solution



# Integrated Droop Response System



Single Cycle Detect Time


Multi-Threshold Detection

<3 Cycles Response

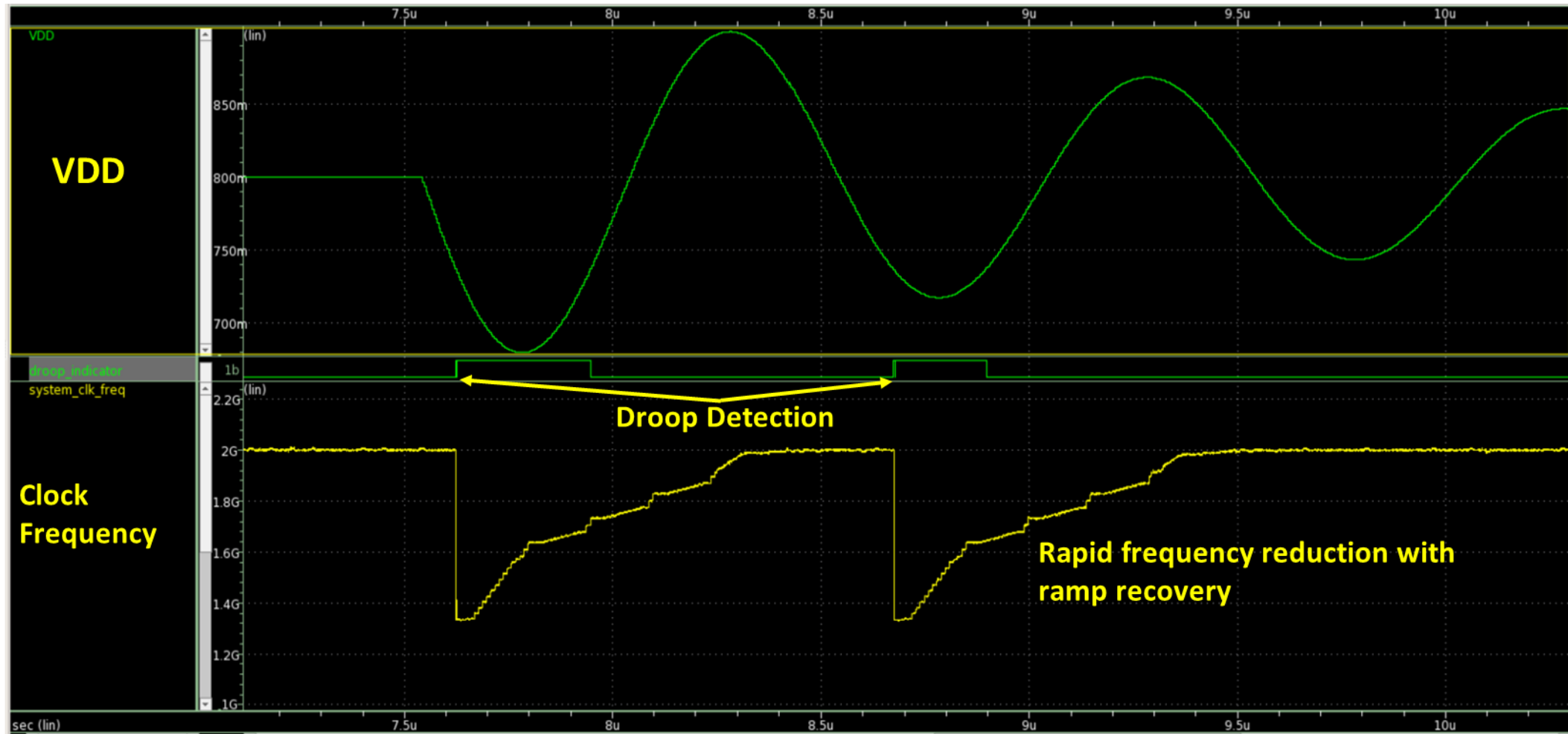
Programmable Ramp Response

Core VDD Only

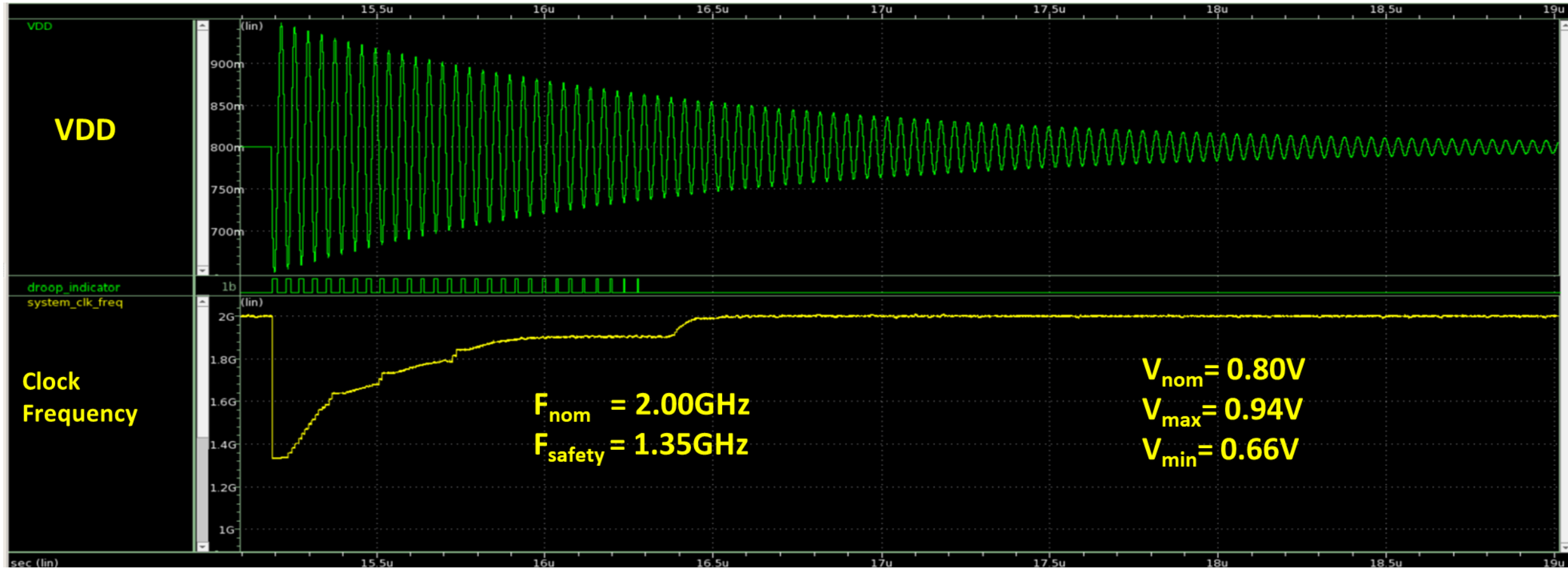
Advanced Droop Telemetry

 Droop Injector is for test chip and verification purposes

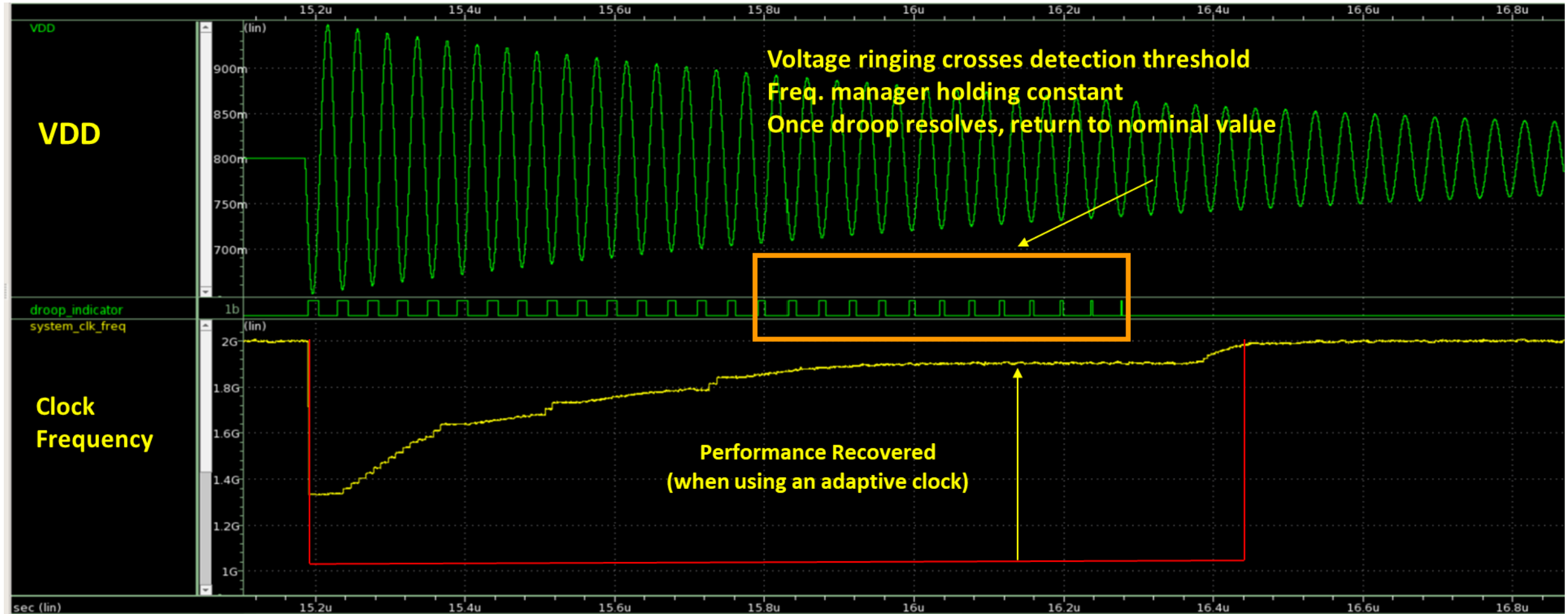
# Simulation: 120mV Droop, 1MHz



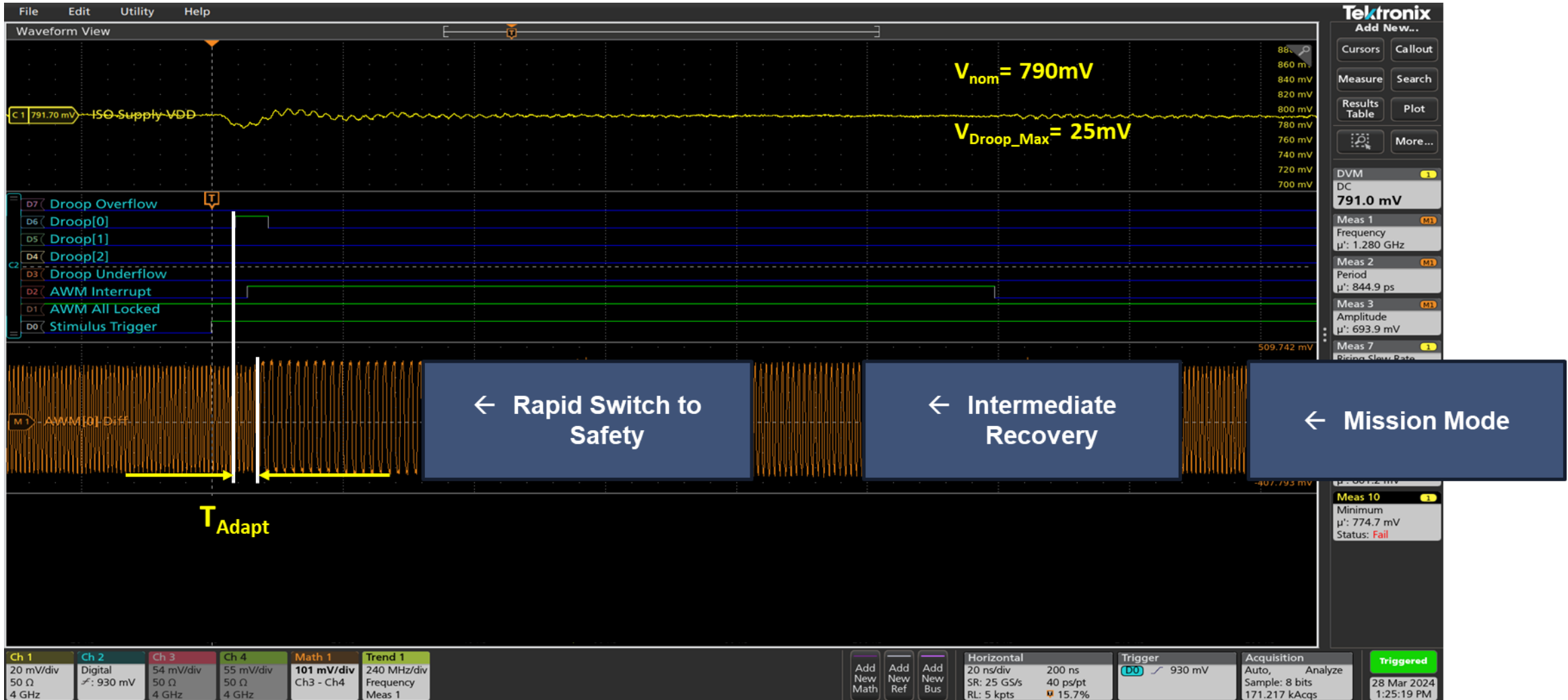
# Simulation: RW 140mV Droop, 25MHz



# Simulation: RW 140mV Droop, 25MHz



# Test Chip: Active Droop Mitigation





# 5 Keys to Active Droop Mitigation

- |   |   |   |   |
|---|---|---|---|
| 1 | <b>Fast Detect and Adapt Time</b>               | → | High-speed droop detection with rapid glitch-free frequency reduction   |
| 2 | <b>Intelligent Clock Frequency Management</b>   | → | Intermediate recovery frequencies to maximize system performance and smooth ramped recovery to prevent self-induced droop |
| 3 | <b>Flexible and Programmable Droop Response</b> | → | Programmable detection thresholds and clock recovery behavior to optimize response to varying droop profiles              |
| 4 | <b>Observability</b>                            | → | Advanced telemetry for droop characterization and PDN behavior  |
| 5 | <b>Turnkey Solution</b>                         | → | Tightly-coupled droop mitigation and detection IP for simplified deployment in various SoC designs                        |

# Summary

1

**Voltage droop is a real and growing problem for large SoCs**

2

**Unmitigated droop will impact power, performance, and reliability**

3

**Active droop mitigation will compliment passive techniques to further recover power, performance and reliability**



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